RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	
0x00100204	
0x00100208	
0x0010020C	

Branch Table

0x00100300	
0x00100304	
0x00100308	
0x0010030C	

ARM Binary (shown disassembled)

0x00100400	
0x00100404	
0x00100408	
0x0010040C	
0x00100410	
0x00100414	

first pass

second pass

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	
0x00100208	
0x0010020C	

Branch Table

0x00100300	0
0x00100304	
0x00100308	
0x0010030C	

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	
0x00100408	
0x0010040C	
0x00100410	
0x00100414	

first pass

second pass

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	
0x0010020C	

Branch Table

0x00100300	0
0x00100304	0
0x00100308	
0x0010030C	

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	
0x0010040C	
0x00100410	
0x00100414	

first pass

second pass

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE 0
0x00100410	
0x00100414	

first pass

second pass

Branch table row: *0x00100208 + 0x04 = 0x0010020C*

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE 0
0x00100410	CMP R3, R0
0x00100414	BEQ 0

first pass

second pass

Branch table row: *0x0010020C - 0x08 = 0x00100204*

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE 0
0x00100410	CMP R3, R0
0x00100414	BEQ 0

first pass

second pass

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE 0
0x00100410	CMP R3, R0
0x00100414	BEQ 0

first pass

second pass

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE 0
0x00100410	CMP R3, R0
0x00100414	BEQ 0

first pass

second pass

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE 0
0x00100410	CMP R3, R0
0x00100414	BEQ 0

first pass

second pass

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

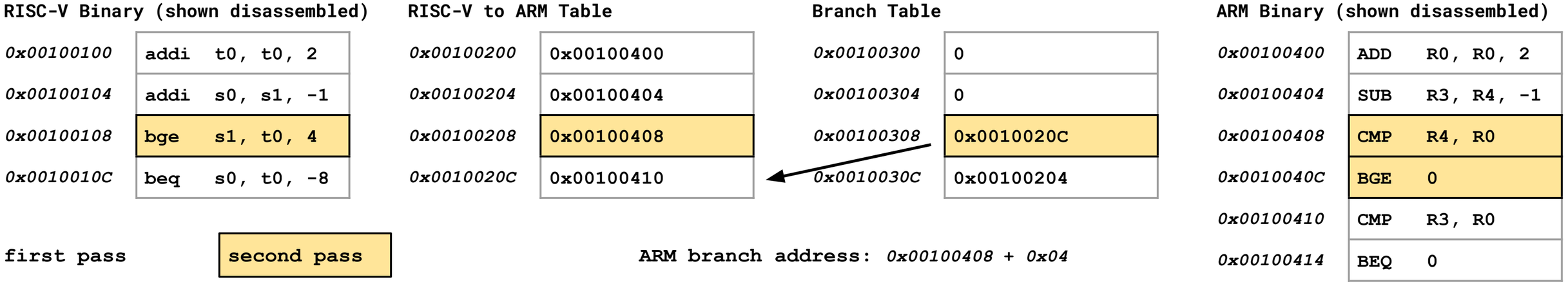
ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE 0
0x00100410	CMP R3, R0
0x00100414	BEQ 0

first pass

second pass

ARM branch address: *0x00100408 + 0x04*


RISC-V Binary (shown disassembled)
0x00100100 addi t0, t0, 2
0x00100104 addi s0, s1, -1
0x00100108 bge s1, t0, 4
0x0010010C beq s0, t0, -8
RISC-V to ARM Table
0x00100200 0x00100400
0x00100204 0x00100404
0x00100208 0x00100408
0x0010020C 0x00100410
Branch Table
0x00100300 0
0x00100304 0
0x00100308 0x0010020C
0x0010030C 0x00100204
ARM Binary (shown disassembled)
0x00100400 ADD R0, R0, 2
0x00100404 SUB R3, R4, -1
0x00100408 CMP R4, R0
0x0010040C BGE 0
0x00100410 CMP R3, R0
0x00100414 BEQ 0
first pass
second pass
ARM branch address: 0x00100408 + 0x04
ARM branch target: 0x00100410

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE 0
0x00100410	CMP R3, R0
0x00100414	BEQ 0

first pass

second pass

ARM branch address: *0x00100408 + 0x04*

ARM branch target: *0x00100410*

ARM branch offset: *0x00100410 - (0x00100408 + 0x04) - 0x08*

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE -0x04
0x00100410	CMP R3, R0
0x00100414	BEQ 0

first pass

second pass

ARM branch address: *0x00100408 + 0x04*

ARM branch target: *0x00100410*

ARM branch offset: *0x00100410 - (0x00100408 + 0x04) - 0x08 = -0x04*

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE -0x04
0x00100410	CMP R3, R0
0x00100414	BEQ 0

first pass

second pass

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

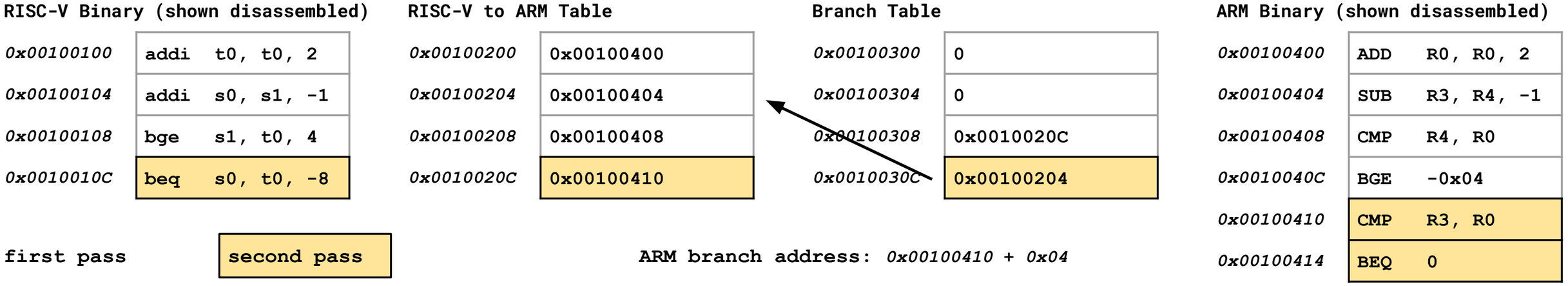
ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE -0x04
0x00100410	CMP R3, R0
0x00100414	BEQ 0

first pass

second pass

ARM branch address: *0x00100410 + 0x04*


RISC-V Binary (shown disassembled)
0x00100100 addi t0, t0, 2
0x00100104 addi s0, s1, -1
0x00100108 bge s1, t0, 4
0x0010010C beq s0, t0, -8
RISC-V to ARM Table
0x00100200 0x00100400
0x00100204 0x00100404
0x00100208 0x00100408
0x0010020C 0x00100410
Branch Table
0x00100300 0
0x00100304 0
0x00100308 0x0010020C
0x0010030C 0x00100204
ARM Binary (shown disassembled)
0x00100400 ADD R0, R0, 2
0x00100404 SUB R3, R4, -1
0x00100408 CMP R4, R0
0x0010040C BGE -0x04
0x00100410 CMP R3, R0
0x00100414 BEQ 0
first pass
second pass
ARM branch address: 0x00100410 + 0x04
ARM branch target: 0x00100404

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE -0x04
0x00100410	CMP R3, R0
0x00100414	BEQ 0

first pass | **second pass**

ARM branch address: *0x00100410 + 0x04*

ARM branch target: *0x00100404*

ARM branch offset: *0x00100404 - (0x00100410 + 0x04) - 0x08*

RISC-V Binary (shown disassembled)

0x00100100	addi t0, t0, 2
0x00100104	addi s0, s1, -1
0x00100108	bge s1, t0, 4
0x0010010C	beq s0, t0, -8

RISC-V to ARM Table

0x00100200	0x00100400
0x00100204	0x00100404
0x00100208	0x00100408
0x0010020C	0x00100410

Branch Table

0x00100300	0
0x00100304	0
0x00100308	0x0010020C
0x0010030C	0x00100204

ARM Binary (shown disassembled)

0x00100400	ADD R0, R0, 2
0x00100404	SUB R3, R4, -1
0x00100408	CMP R4, R0
0x0010040C	BGE -0x04
0x00100410	CMP R3, R0
0x00100414	BEQ -0x18

first pass | **second pass**

ARM branch address: *0x00100410 + 0x04*

ARM branch target: *0x00100404*

ARM branch offset: *0x00100404 - (0x00100410 + 0x04) - 0x08 = -0x18*